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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,790	01/15/2004	Thomas Joseph Beacom	ROC920030257US1	5443

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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,790	BEACOM ET AL.	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Final Rejection

Response to Arguments

1. Applicant's arguments, filed November 24, 2006, with respect to the Title have been fully considered and are persuasive. The objection to the Specification has been withdrawn.

2. Applicant's arguments, filed November 24, 2006, with respect to the rejections under 35 USC 112 have been fully considered and are persuasive. The rejections under 35 USC 112 have been withdrawn.

3. Applicant's arguments with respect to claims 1, 5-7, and 10-13 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6, 7, 10, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vorbach (U.S. Patent No. 6,697,979) in view of Kromer (U.S. PGPub 2004/0255099), further in view of Shidla et al. (U.S. PGPub 2005/0055674).

As in claims 1 and 7, Vorbach et al. teaches a method and an apparatus comprising:

detecting an event that would cause cycles to be idle in a processor *(column 4 line 65 through column 5 line 10, and column 10 lines 49-53, where it is inherent that a event be detected in order to cause a processor IDLE cycle)*;

selecting diagnostic instructions based on a number of the cycles that would be idle *(column 5 lines 7-10)*;

issuing the diagnostic instructions to the processor during the cycles that would be idle *(column 4 line 65 through column 5 line 10)*; and

comparing a result of the diagnostic instructions with a pre-computed result *(column 3 lines 48-54, where it is interpreted that the setpoint result is pre-computed)*.

However, Vorbach et al. fails to teach of specific operand processes and saving of intermediate results. Kromer teaches of using initial values in a first diagnostic instruction and incrementing operands of respective next diagnostic instructions, wherein the respective next diagnostic instructions use output of respective previous instructions as input *(paragraphs [0032]-[0040], where the term "incrementing" as read in light of the Applicant's Specification on page 13 in lines 21-23 is interpreted as any type of instruction operation carried out on the result)*. Shidla et al. teaches if the diagnostic instructions partially complete during the cycles that would be idle, saving an intermediate result and retrieving the intermediate result on a next idle cycle sequence *(paragraphs [0027] and [0029], where an intermediate result from a*

diagnostic operation during an idle cycle must be saved in order to use the intermediate result during a next idle cycle for fault checking).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the using of results as input as taught by Kromer in the invention of Vorbach. This would have been obvious because the invention of Kromer reduces the amount of circuitry needed to carry out processing, which reduces the cost and increases the efficiency of such a computer system *(paragraph 0014]).* Further, it is well known in the art to have an instruction compute a value and then use that computed value in a next instruction, regardless of the application. The claimed invention as interpreted by the Examiner relates only to instructions that are placed one after the other in this manner in a diagnostic system, which is not interpreted as being novel over the applied prior art.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the intermediate result as taught by Shidla et al. in the combined invention of Vorbach et al. and Kromer. This would have been obvious because utilizing idle cycles in a processor for fault checking as taught by Shidla et al. reduces cost and preserves system performance in a fault tolerant system *(paragraph [0006]).*

As in claim 6, Vorbach et al. discloses the event comprises a task switch *(column 5 lines 1-2, where the switching from a program task running on a computer to no program running implies a task switch causing idle processor cycles).*

As in claim 10, Vorbach teaches of a processor comprising:

an issue unit to detect an event that would cause cycles to be idle in the processor and issue diagnostic instructions during the cycles that would be idle to a pipeline *(column 4 line 65 through column 5 line 10, and column 10 lines 49-53, where it is inherent that a event be detected in order to cause a processor IDLE cycle)*, wherein a first diagnostic instruction uses initial values *(inherent)*;

a compare unit to compare the pre-computed result with a result of the diagnostic instructions *(column 3 lines 48-54, where it is interpreted that the setpoint result is pre-computed)*.

However, Vorbach fails to teach of result of a previous instruction being input to an immediate subsequent instruction and a write back unit. Kromer teaches of an increment unit to increment operands of respective next diagnostic instructions, wherein the respective next diagnostic instructions use output of respective previous instructions as input *(paragraphs [0032]-[0040], where the term "incrementing" as read in light of the Applicant's Specification on page 13 in lines 21-23 is interpreted as any type of instruction operation carried out on the result)*. Shidla et al. teaches of a write back unit to save an intermediate result of the diagnostic instructions and retrieve the intermediate result on a next idle cycle sequence if the diagnostic instructions partially complete during the cycles that would be idle *(paragraphs [0027] and [0029], where an intermediate result from a diagnostic operation during an idle cycle must be saved in order to use the intermediate result during a next idle cycle for fault checking; any memory used to save the result is interpreted as a write back unit)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the using of results as input as taught by Kromer in the invention of Vorbach. This would have been obvious because the invention of Kromer reduces the amount of

circuitry needed to carry out processing, which reduces the cost and increases the efficiency of such a computer system *(paragraph 0014])*. Further, it is well known in the art to have an instruction compute a value and then use that computed value in a next instruction, regardless of the application. The claimed invention as interpreted by the Examiner relates only to instructions that are placed one after the other in this manner in a diagnostic system, which is not interpreted as being novel over the applied prior art.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the intermediate result as taught by Shidla et al. in the combined invention of Vorbach et al. and Kromer. This would have been obvious because utilizing idle cycles in a processor for fault checking as taught by Shidla et al. reduces cost and preserves system performance in a fault tolerant system *(paragraph [0006])*.

As in claim 11, Vorbach teaches the issue unit is further to select the diagnostic instructions based on a number of the cycles *(column 5 lines 7-10)*.

As in claim 13, Vorbach teaches the event comprises a task switch *(column 5 lines 1-2, where the switching from a program task running on a computer to no program running implies a task switch causing idle processor cycles)*.

* * *

5. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vorbach et al., in view of Kromer, further in view of Shidla et al., further in view of Zilka (U.S. PGPub 2003/0061383).

As in claims 5 and 12, the combined invention of Vorbach et al., Kromer, and Shidla et al. teaches of an event causing a processor to idle. However, the combined invention of Vorbach et al., Kromer, and Shidla et al. fails to teach of processor idling in response to a cache miss. Zilka teaches of a processor idling in response to a cache miss *(paragraph [0012])*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the cache miss event response as taught by Zilka in the combined invention of Vorbach et al., Kromer, and Shidla et al. This would have been obvious because the invention of Zilka reduces the power consumption necessary to operate a computer system *(paragraph [0003])*.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 6,360,336 Christensen et al. discloses idle testing with resuming of testing during subsequent idle cycles.

U.S. PGPub 2003/0149546 Kim discloses resumption of diagnostics during processor idle.

U.S. PGPub 2004/0181656 Stern et al. discloses testing during processor idle.

GB 1,247,746 A IBM discloses testing during idle cycles.

7. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
1/3/2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER